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CSS 422

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Homework Problem Set #3

From <https://faculty.washington.edu/aberger/CSS422W09/Homework/Homework%203/CSS422W09HW3.htm>

1. Consider a processor with a 20-bit address range and an 8-bit wide data bus. The memory system will consist of 1 MB static ram parts (SRAM) with a worst-case read or write cycle access time of 35 nanoseconds. The SRAMs are organized as 128K by 8.
2. How many 128K byte memory pages are there in the processor's address space?  
   8 pages (128K \* 8 = 1 MB)
3. What are the memory address ranges, in hexadecimal, for each page of memory?

|  |  |
| --- | --- |
| Page | Address Range |
| 0 | 0x00000 – 0x1FFFF |
| 1 | 0x20000 – 0x3FFFF |
| 2 | 0x40000 – 0x5FFFF |
| 3 | 0x60000 – 0x7FFFF |
| 4 | 0x80000 – 0x9FFFF |
| 5 | 0xA0000 – 0xBFFFF |
| 6 | 0xC0000 – 0xDFFFF |
| 7 | 0xE0000 – 0xFFFFF |

1. Assuming that the processor will be designed to run with 0 wait states, what is the maximum clock frequency that we could use with these memory chips?  
   35 ns = 1/35 GHz or 28 MHz
2. Design the logic required for the ADDRESS DECODER BLOCK of Figure 6.16. Assume that memory is required at pages 0, 4 and 7.

Truth table for a 3:8 decoder:

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| A17 | A18 | A19 |  |  |  |  |  |  |  |  |  |  |  |
| 0 | 0 | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| 0 | 0 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| 0 | 1 | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| 0 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| 1 | 0 | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| 1 | 0 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| 1 | 1 | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| 1 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| 0 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| 0 | 1 | 0 | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| 0 | 1 | 1 | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| 1 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 1 |
| 1 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| 1 | 1 | 0 | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| 1 | 1 | 1 | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 |
| 0 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| 0 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| 0 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| 0 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| 1 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| 1 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| 1 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| 0 | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| 0 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| 0 | 1 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| 1 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 1 |
| 1 | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| 1 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| 1 | 1 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 |

1. You have a memory device with the following pins:

* A0 – A16 (128K addressable bytes)
* D0 – D15 (16-bit data bus)

It will be used in a memory system for a computer with the following specifications:

* 20-bit address bus
* 32-bit data bus
* Memory at pages 0, 1, and 7

1. How many addressable memory locations are in each memory device?  
   128K
2. How many bits of memory are in each memory device?  
   1 megabit (1,048,576 bits)
3. What is the address range, in hex, covered by each memory device in the computer's address space? You may assume that each page of memory is the same size as the address range of one memory device.  
   Page size: 128K ()

|  |  |
| --- | --- |
| Page | Address Range |
| 0 | 0x00000 – 0x1FFFF |
| 1 | 0x20000 – 0x3FFFF |
| 7 | 0xE0000 – 0xFFFFF |

1. What is the total number of memory devices required in this memory design?  
   6 devices. Two 16-bit devices \* 3 addressable pages.
2. Why would a memory system design based upon this type of a memory device not be capable of addressing memory locations at the byte level? discuss the reason for your answer in a sentence or two.  
   A 20-bit address bus lacks the capacity to address every byte in a memory system with a 32-bit data bus and 8 pages of memory, due to the 3 address lines required for paging. 23 address bits would be required in this case.
3. Draw the truth table that corresponds to the hardware algorithm represented by the diagram. Simplify it, and then draw the entire circuit with the gate equivalent circuit replacing the truth table.

Truth table:

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| A | B | C | a | b | c |
| 0 | 0 | 0 | 1 | 1 | 0 |
| 0 | 0 | 1 | 1 | 1 | 1 |
| 0 | 1 | 0 | 0 | 0 | 0 |
| 0 | 1 | 1 | 0 | 0 | 0 |
| 1 | 0 | 0 | 1 | 0 | 1 |
| 1 | 0 | 1 | 0 | 1 | 1 |
| 1 | 1 | 0 | 0 | 0 | 1 |
| 1 | 1 | 1 | 1 | 0 | 0 |

K-maps:

a = 'A'B + ABC + 'B'C

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| AB/C | 00 | 01 | 11 | 10 |
| 0 | 1 |  |  | 1 |
| 1 | 1 |  | 1 |  |

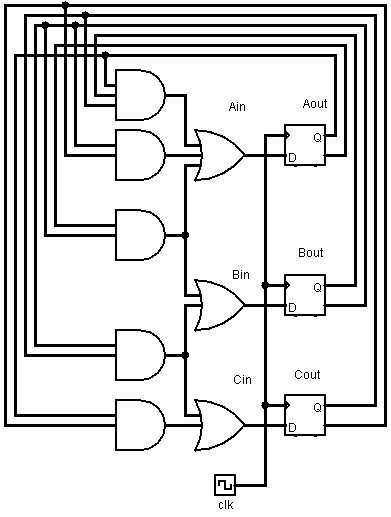
b = 'A'B + 'BC

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| AB/C | 00 | 01 | 11 | 10 |
| 0 | 1 |  |  |  |
| 1 | 1 |  |  | 1 |

c = 'BC + A'C

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| AB/C | 00 | 01 | 11 | 10 |
| 0 |  |  | 1 | 1 |
| 1 | 1 |  |  | 1 |

Circuit:



4- What is the word value of the data in memory location $4000 when the program is just about to loop back to the beginning and start over again?  
0x4515

Extra credit: "Creatures from the id" was a famous plot line from what classic science fiction motion picture?  
The Forbidden Planet